PLUS 4 Test

#5243(4)

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GENERAL DISCRIPTION

1. INITIALISE

- ° CPU - Stack and flags
- ° Bank set - LO / Cartridge 1 (DIAG)
  HI / Kernal (Normal)
- ° I/O ports - Preset
- ° TED chip - Initialize reg's
- ° RAM - Set memory size (16,32,64K)
- ° Pass count - Clear
- ° Screen - Initial display

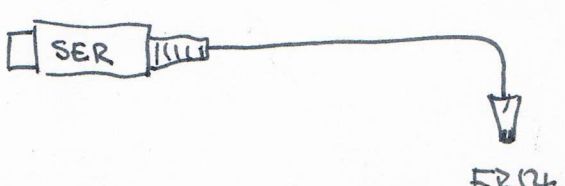
2. MAIN

Preform each test, check for error, display the result. Also included in the main routine is the doun load routine for moving the DIAG. program from cartridge ROM to RAM area.

3. FINAL ROUTINE

Incriment the pass count, go back to initialize routine (entry at screen clear), and repeat the test.

für C16 / C116



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4. TEST ROUTINES

(1) RAM test

(2) ROM check sum

(3) I/O test

(4) Timer
(5) Interrupt
(6) Sound
(7) Screen display

] TED reg. test

5. SUB ROUTINES

(1) Screen clear

(2) Titile/count display

(3) Message/disp. addr. set

(4) Display message

(5) Display "OK" message

(6) Display callent addr./data (in ROM)

(7) Display callent addr./data (in RAM)

(8) Hex-dec. converter / screen code (in ROM)

(9) Hex-dec. converter / screen code (in RAM)

(10) Time delay

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6. ERROR ROUTINE

Display "NG" message with charactor color red, flash.

(1) RAM test error

Display error addr. , write data and read data.

(2) Other test errors (ROM, I/O, Timer, Interrupt, etc.)

Display error code. (* See error code list)

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DETAIL DISCRIPTION EACH TEST

1. RAM TEST

	addr.
Zero page	02H - FFH
Stack page	100H - 2FFH
System RAM	200H - 7FFH
Color RAM	800h - BFFH
Video RAM	C00H - FFFH
User's RAM 1	1000H - 3FFFH
User's RAM 2	4000H - 7FFFH
User's RAM 3	8000H - BFFFH
User's RAM 4	C000H - FFFFH

(16K System, execute only user's RAM 1 test.)

(32K System, execute user's RAM 1,2 test)

Each RAM cell is written to and the a read verify is performed on each. The data patterens used for testing the RAM is 55H, AAH and the low byte address of that RAM location. After writing to RAM, there is a delay for the DRAM cycle of 0.002sec before reading the RAM. This will test for DRAM refreshing.

Durring the System RAM / User's RAM test, the screen will display the HI address byte value currently under test.

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2. ROM TEST

1) KERNAL / BASIC ROM

LO ROM	addr. 8000H - BFFFH	value	80H
HI ROM	C000H - FCFFH		C0H
	+		(skip I/O, TED chip)
	FF40H - FFFFH		

Display addr. HI byte to the screen durring test.

2) FUNCTION LO/HI ROM

LO ROM	addr. 8000H - BFFFH	value	○ H
HI ROM	C000H - FBFFH		○ H
			(skip no bankig KERNAL, I/O, TED chip)

* ROM check sum : (ADD with CARRY and ADD LAST CARRY), compare correct value in data table.

* When finished KERNAL / BASIC ROM test, check memory size (look for top of RAM flag), and skip next FUNCTION ROM test except 64K system (C-Plus 4).

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3. I/O TEST

At first, check if JIG key bouad cable is connected or not. If it is, use the check routine for the 6529 port on host PCB. In case of no connection, use to the check routine for the 6529 port on JIG PCB, and skip key port test. Also, display "-K" message to indicate no connection.
(Refer. : Screen format sheets)

* CAUTION :

Please verify the when the JIG key bouad cable is connected or not, that the correspounding display message is correct. If not, then check the connection of the JIG key bouad cable.

1) CASSETTE TEST

- ° Write -- Read
- ° Motor -- Sense

2) KEY PORT TEST

3) SERIAL TEST

- ° Data out -- Data in
- ° CLK out -- CLK in

4) JOY PORT 1 TEST

- ° Pin 1 - 4
- ° Fire

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5) JOY PORT 2 TEST

° Pin 1 - 4

° Fire

When finished joy port 2 test, check memory size (look for top of RAM flag), and skip next user's port test except 64K system (C-Plus 4).

6) USER'S PORT TEST

(1) 6529 port test

(2) 6551 baud rate generator test

300 baud and 1200 baud count RxC value, and check with in the limits of correct value. Limits, that with software time (ioss time of software counting), ± 33.8 . Count is done 16 times.

* Refer. next sheet for how to count RxC value.

(3) 6551 DTR - DSR

(4) 6551 RTS - DCD

(5) 6551 transmit and receive data

Check transmit and receive data correctly.

Set mode at : Even parity

2 stop bit

Data length 7 bits

And check to change baud rate.

(300 / 600 / 1200 / 2400 / 4800 / 9600 baud)

7) EXTERNAL AUDIO IN / CARTRIDGE 2 LO,HI LINE TEST

Test will start will bank select for cartridge 2 enabled. The cartridge HI (C000H) and LO (8000H) will be switched at APX 1KHz rate. The duration of this switching is about 2.5sec. If the 1KHz sound can be heard from the external audio in line then result is okay.

(Refer : TED series DIAGNOSTIC schematics)

4. TIMER TEST

Perform timer test in the following; timer 1, timer 2 and timer 3.

First preset the timers with full value and next read value, also read it after an interval time and compare the former to the latter. If there is a difference between them, then result is okay.

5. INTERRUPT TEST

Perform this test in the following; timer 1 int., timer 2 int., timer 3 int. and raster int.

After occurance of IRQ, the IRQ routine flag is checked for result.

6. SOUND TEST

° VOICE#1 / VOICE#2

First start with voice#1, and then do voice#2 after about 0.4sec delay. Then turn off both voice#1 and #2.

To make sound :

Perform the test in the following; volume set, freq. LO set, freq. HI set and enable bit set.

To turn off :

Freq. LO = 0, freq. HI = 0, enable bit = 0 and volume = 0 .

Change freq./vol. to the following settings.

1) Freq. = C4 Vol. = 04H (1/4 full)

2) E4 08H (1/2 full)

3) G4 0CH (3/4 full)

4) C5 0FH (full)

° NOISE

Set at freq. A4 / vol. full and make noise.

Turn off after about 1.5sec.

The way to make noise on and off is same for voise #1 and #2.

7. SCREEN DISPLAY

1) BACK GROUND AND BORDOR COLOR

Assortment eight(8) back groung colors (color code 0 - 7) with eight(8) bordor colors (color code 8-FH).

Change eight(8) back ground colors for one(1) bordor color and repeat that for each change. Timing for change of back ground colors is about 0.1sec.

But, each luminance is 0.

2) COLOR AND LUMINANCE BARS

Show bar of each five(5) RVS space with assortment sixteen (16) colors X eight(8) luminances.

On the screen ; The vertical is 0-FH color change.

The horizontal is 0-7 luminance change.

(Refer to screen format)

3) FLASH TEST

Display "FLASH !" with sixteen(16) colors on screen, and be flashed.

Color ; 0-FH from upper left side toward lower right side.

But, each luminance is 1.

(Refer to screen format)

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TED SERIES SYSTEM I/O MAP

ADDR	DESCRIPTION	7	6	5	4	3	2	1	0
00H	7501 PORT (DATA DIR. REG.)	0 IN	0 IN	N.C. (0 IN)	0 IN	1 OUT	1 OUT	1 OUT	1 OUT
01H	7501 PORT (OUTPUT REG.)	SER. DATA IN	SER. CLK IN	N.C.	CAS READ	CAS $\overline{\text{MTR}}$	SER. $\overline{\text{ATN}}$	CAS $\overline{\text{WRITE}}$ SER. $\overline{\text{CLK OUT}}$	SER. $\overline{\text{DATA OUT}}$
FD00H	ACIA (6551) DATA	W TRANSMIT DATA REGISTOR R RECEIVER DATA REGISTOR							
FD01H	ACIA (6551) STATUS	W (RESET) R STATUS							* REFER 6551 SPEC
FD02H	ACIA (6551)	COMMAND							* REFER 6551 SPEC
FD03H	ACIA (6551)	CONTROL							* REFER 6551 SPEC
FD10H	6529 PORT (USER'S PORT ETC.) (DIAG ONLY)	P7	P6	P5	P4	P3	P2 CAS $\overline{\text{SENSE IN}}$	P1	P0 (RxC)
FD30H	6529 PORT (KEY PORT OUT)	K7 OUT	K6 OUT	K5 OUT	K4 OUT	K3 OUT	K2 OUT	K1 OUT	K0 OUT
(FD40H)	6529 PORT (DIAG JIG PORT	K7 OUT	K6 OUT	K5 OUT	K4 OUT	K3 OUT	K2 OUT	K1 OUT	K0 OUT

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ADDR	DESCRIPTION	7	6	5	4	3	2	1	0
FDDOH ~ FDDFH	FPLA (BANKING)	(*REFER TED SPEC BANKING MAP)							
FF08H	8360/7360 KEY LATCH REG.	K7 IN J2 FIRE	K6 IN J1 FIRE	K5 IN	K4 IN	K3 IN J1/J2 -4	K2 IN J1/J2 -3	K1 IN J1/J2 -2	K0 IN J1/J2 -1

TED SERIES DIAG. I/O GATE ON/OFF SW

(CAS MOTOR LINE / SER. ATN LINE)

* REFER SCHEMATICS

GATE 1	KEY PORT	MTR = 0	ATN = 0
GATE 2	USER'S PORT 6529	MTR = 1	ATN = 0
GATE 3	JOY 1	MTR = 1	ATN = 1
GATE 4	JOY 2	MTR = 0	ATN = 1

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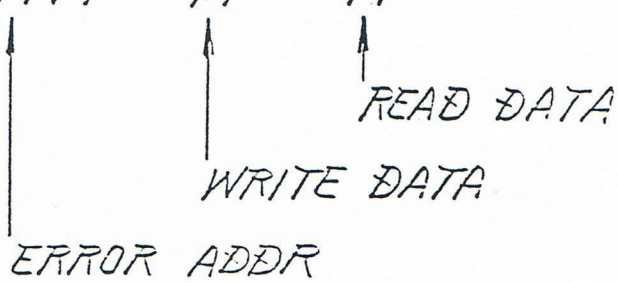
ERROR MESSAGE , ERROR CODE LIST

○ RAM ERROR

NG FFFF FF FF



○ OTHER ERRORS

NG X.

TEST	CODE	ERROR
ROM TEST	1	LO ROM (BASIC), CHECK SUM IS NOT CORRECT.
	2	HI ROM (KERNAL), CHECK SUM IS NOT CORRECT.
	3	FUNCTION LO, CHECK SUM IS NOT CORRECT.
	4	FUNCTION HI, CHECK SUM IS NOT CORRECT.

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TEST	CODE	ERROR
I/O TEST	1	CAS WRITE → CAS READ
	2	CAS MOTOR → CAS SENSE
	3	KEY PORT
	4	SER. DATA OUT → SER. CLK IN
	5	SER. CLK OUT → SER. DATA IN
	6	JOY 1 PIN 1 — PIN 4
	7	JOY 1 PIN 6 (FIRE), PIN 8
	8	JOY 2 PIN 1 — PIN 4
	9	JOY 2 PIN 6 (FIRE), PIN 8
	A	USER'S PORT 6529
	B	BAUD RATE GENERATOR (6551) 300 BAUD
	C	BAUD RATE GENERATOR (6551) 1200 BAUD
	D	DTR → DSR (6551)
	E	RTS → DCD (6551)
	F	TRANSMIT AND RECEIVE DATA (6551)

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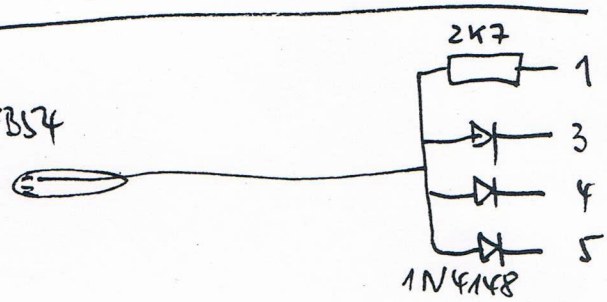
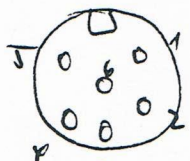
TEST	CODE	ERROR
TIMER TEST	1	TIMER 1
	2	TIMER 2
	3	TIMER 3
INTERRUPT TEST	1	RASTER IRQ
	2	TIMER 1 IRQ
	3	TIMER 2 IRQ
	4	TIMER 3 IRQ

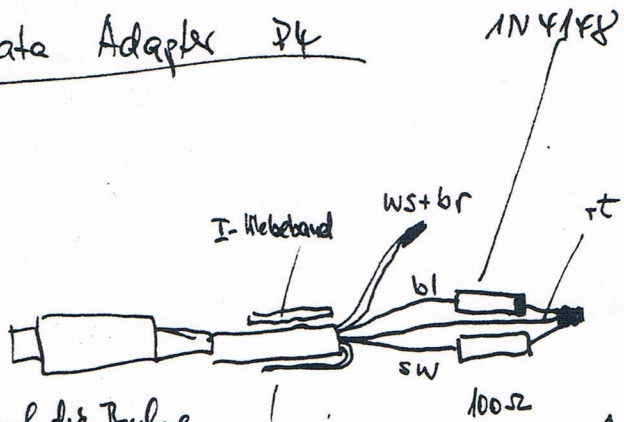
DIAGNOST P4 C16/M6





auf die Buchse gesehen

Data Adapter P4



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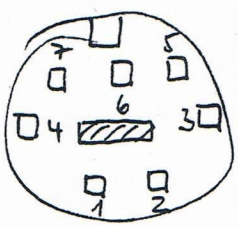
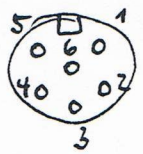


		A	B
1	Masse	gelb	se (se)
2	+5V	grün	gn (gn)
3	Motor	ws	ws (ws)
4	Read	rt	rt (rt)
r	Write	schwarz	sw. (sw)
6	Schalter	blau	bl. (bl)
7	Masse	braun	br (br)

P4 Diagnost USERPORT + SER

auf den USER-PORT gesehen

G	USERPORT	SERIELL	
sw	B	5	sw
br	5	3	br
rt	K	4	se



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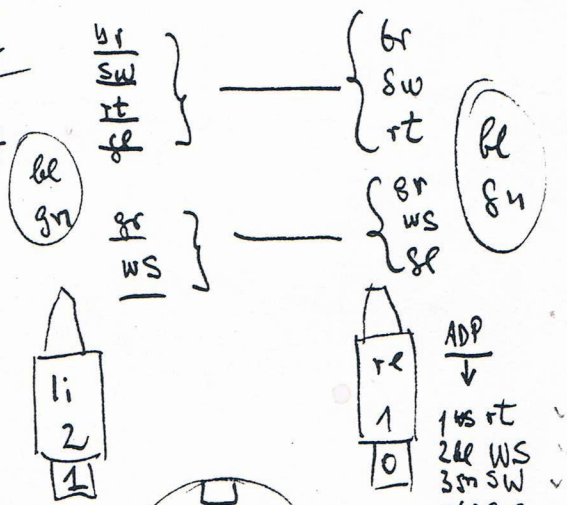
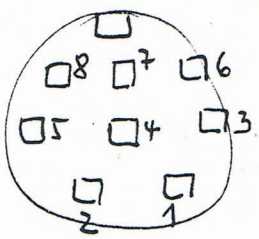
Joy 1+2

Diag P4





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